



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,013	09/12/2003	Nathan N. Strader	03-0939	6798
7590	12/10/2004		EXAMINER	
Intellectual Property Law Department LSI Logic Corporation Mail Stop D-106 1551 McCarthy Boulevard Milpitas, CA 95035				WALLING, MEAGAN S
		ART UNIT		PAPER NUMBER
		2863		
DATE MAILED: 12/10/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/661,013	STRADER, NATHAN N.
	Examiner	Art Unit
	Meagan S Walling	2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 September 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-3,5,8-10,12,14,19 and 20 is/are rejected.
7) Claim(s) 4,6,7,11,13 and 15-18 is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 12 September 2003 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 09122003.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____ .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3, 5, 8, 9, 12, 14, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Okabe et al. (US 6,799,130).

Regarding claim 1, Okabe et al. teaches providing a semiconductor wafer (see Fig. 2); generating a map of points of interest proximate to an edge of the semiconductor wafer (column 5, line 28); supplying the points of interest to the review tool in automatic succession (column 5, lines 37-40 and column 6, lines 1-4) instructing the review tool to capture images at the points of interest (column 5, lines 20-25) automatically storing the captured images (column 5, lines 24-25) and correlating the captured images with the points of interest (column 5, lines 29-30).

Regarding claim 2, Okabe et al. teaches identifying the points of interest with location identifiers for fake defects at the point of interest (column 4, lines 50-53 and column 5, lines 26-30).

Regarding claim 3, Okabe et al. teaches generating context information for the captured images identifying the semiconductor wafer (column 5, lines 37-38); and correlating the captured images with the context information (column 5, lines 29-30).

Regarding claim 5, Okabe et al. teaches providing a semiconductor wafer (see Fig. 2); generating points of interest proximate to an edge of the semiconductor wafer by identifying fake defects with fake defect identifiers (column 4, lines 50-53 and column 5, lines 28); causing the review tool to capture images at the points of interest by instructing the review tool to capture the images at the fake defects identified by the fake defect identifiers (column 5, lines 20-25); and storing the captured images (column 5, lines 24-25).

Regarding claim 8, Okabe et al. teaches generating context information including information identifying the semiconductor wafer (column 5, lines 37-38); and correlating the captured images with the context information (column 5, lines 26-30).

Regarding claim 9, Okabe et al. teaches providing a semiconductor wafer (see Fig. 2) generating context information including information identifying the semiconductor wafer (column 5, lines 37-38); generating a map of points of interest proximate to an edge of the semiconductor wafer (column 5, line 28) instructing the review tool to capture images at the points of interest (column 5, lines 20-25); storing the captured images (column 5, lines 24-25); and correlating the captured images with the points of interest and the context information (column 5, lines 26-30).

Regarding claim 12, Okabe et al. teaches a software tool (Ref. 61) instructing the review tool to capture the images at the points of interest (column 5, lines 20-25); and the software tool correlating the captured images with the points of interest and the context information (column 5, lines 26-28).

Regarding claim 14, Okabe et al. teaches a review tool (Ref. 60) having an image capturing device capable of capturing an image of the semiconductor wafer edge (Ref. 67); a

software tool (Ref. 61) connected to the review tool to supply instructions to the review tool to capture an image at a point of interest on the semiconductor wafer edge and to receive the captured image from the review tool (column 5, lines 20-25); and a database connected to the software tool (Ref. 62) to receive and store the captured image from the software tool and context information identifying the semiconductor wafer, the context information being correlated with the captured image (column 5, lines 26-30 and 37-38).

Regarding claim 20, Okabe et al. teaches that the instructions supplied from the software tool to the review tool include a plurality of points of interest at which the review tool captures a plurality of images in automatic succession (column 5, lines 37-40 and column 6, lines 1-4); and the software tool automatically receives and stores the captured images in the database correlated with the context information for each image (column 5, lines 24-25 and 29-30).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okabe et al. in view of Matsumoto et al. (US 2002/0111038).

Okabe et al. teaches everything claimed in claims 10 and 19 except the limitation of storing the context information in a computer-searchable manner (current claim 10) and that the database, including the context information, is computer-searchable (current claim 19).

Matsumoto et al. teaches storing semiconductor context information in a computer-searchable database (see paragraph 91).

It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Okabe et al. with the teachings of Matsumoto et al. to store the context information in a computer-searchable database. The motivation for making this combination would be to allow the user to quickly find a type of semiconductor based on identifying features stored in the database.

Allowable Subject Matter

3. Claims 4, 6, 7, 11, 13, and 15-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for the indication of allowability of claims 4, 11, and 13 is the inclusion of the limitation that the review tool is incorporated in a semiconductor fabrication system having a plurality of fabrication stations for performing fabrication steps on the semiconductor wafer, the review tool is situated subsequent to a preceding one of the fabrication stations, and the aforementioned context information is first context information, further comprising: generating second context information for the captured images identifying the preceding fabrication station; and correlating the captured images with the second context information. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 6 is the inclusion of the limitation that the review tool captures images of the semiconductor wafer through a view finder and can drive the view finder to an identified defect location, further comprising: supplying the fake defect identifiers to the review tool; and instructing the review tool to drive the view finder to the fake defects identified by the fake defect identifiers and to capture images at the fake defects. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 15 is the inclusion of the limitation that the review tool is capable of capturing the image at a predetermined defect location; the point of interest is indicated by a predetermined fake defect location identified by a fake defect identifier; the instructions supplied from the software tool to the review tool include the fake defect identifier; and the review tool captures the image at the predetermined fake defect location. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 18 is the inclusion of the limitation that the review tool is situation in the fabrication system subsequent to the preceding fabrication station; and the context information further identifies the preceding fabrication station. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

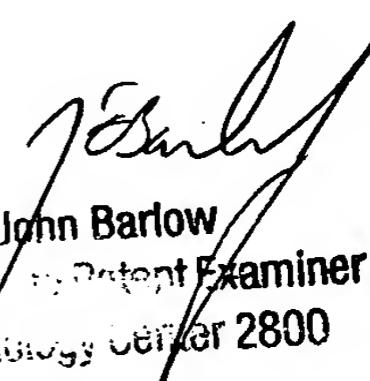
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Meagan S Walling whose telephone number is (571) 272-2283. The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

msw


John Barlow
Supervisory Patent Examiner
Technology Center 2800